REMARKS/ARGUMENTS

In response to the Office Action mailed May 3, 2007, Applicant amends his application and requests reconsideration. No claims are added or cancelled so that claims 1-7 remain pending.

Dependent claims 2-7 were stated to allowable subject to overcoming two rejections pursuant to 35 USC 112, second paragraph. Therefore, there is no further comment on those dependent claims 2-7.

In response to the two rejections pursuant to 35 USC 112, second paragraph, claim 1 has been revised for clarity. Although Applicant does not agree that there was any error or omission in claim 1 as submitted, the claim has been amended in several ways. The beginning of the claim has been reformatted to describe the basic elements of the half-rate clock and data recovery circuit and the interconnections of those basic elements. This amendment is consistent with and supported by Figure 1 of the patent application and the description of that figure in the patent application from page 5, line 21-page 6, line 13. In addition, the elements of the half-rate phase detector described in amended claim 1 are now described with respect to their interconnections and the various signals that are generated and passed from one element to another. These amendments are entirely consistent with the embodiment of Figure 6 of the patent application, which is described in the patent application from page 7, line 5 through page 12, line 22 in both structure and operation.

In view of the comments in one of the rejections regarding the re-timed signal produced by the selector circuit, the operation of the selector circuit is described in somewhat more detail in amended claim 1. This description is supported by the patent application as filed at page 9, in the paragraph beginning in line 6 and, particularly, the description at that page in lines 9-11. In specific response to the second of the rejections pursuant to 35 USC 112, second paragraph, the final two paragraphs of claim 1 have been reorganized for clarity. The one-pulse delay circuit is more clearly described as outputting through-data after generating a delay of one pulse, a feature that inverts the phase comparison polarity. The effect of inserting a one-pulse delay, with respect to the half-rate clock, is a phase inversion as described in the patent application at page 9 in the paragraph beginning in line 12. See, particularly, lines 18-24 on page 9.

Further, the final paragraph of claim 1 is amended to explain that the voltage controlled oscillator is an N-type LC voltage controlled oscillator. As explained extensively

in the patent application, this kind of voltage controlled oscillator was known in the prior art and is known to have improved properties with respect to jitter as compared to an P-type voltage controlled oscillator. However, it is not possible to use the N-type oscillator conventionally, as described in the patent application. Through the use of the one-pulse delay circuit in the invention, an inversion of phase comparison polarity is achieved, enabling the use of that N-type voltage controlled oscillator. This feature and its advantages are described at pages 10-12 of the patent application and summarized in the paragraph beginning in line 16 on page 12. The ability to use the N-type voltage controlled oscillator due to the presence of the one-pulse delay is now more clearly described in the final paragraph of claim 1. This and the other clarifying amendments of claim 1, described above, overcome both rejections pursuant to 35 USC 112, second paragraph.

Claim 1 was rejected as obvious over Friedman et al. (published U.S. patent application 2004/0114702, hereinafter Friedman) in view of Ono et al. (published U.S. patent application 2002/0097075, hereinafter Ono), and further in view of Cai (U.S. patent 6,396,360). This rejection is respectfully traversed.

Cai was cited for the proposition that an N-type LC VCO was known in the prior art. Applicant agrees. The present patent application does not assert that the invention is an N-type LC VCO. Rather, the present invention is directed to an application in which such a VCO is employed. Therefore, no further comment on Cai is necessary or provided.

While it is understood how Figure 5 of Friedman was applied in rejecting the claim 1 that was examined, in view of the clarifications of the claims that application of Friedman can no longer be made. In making the application, there seems to be some confusion at page 2 of the Office Action with respect to the first two bulleted points. In the first instance, it seems to been asserted that Friedman's latches 5111 and 5112 correspond to the first-stage latch circuits. In the second instance, in a comparison that seems to be more accurate, the first-stage latch circuit and the additional first-stage latch circuit are compared to Friedman's latches 5111 and 51112. Even applying that interpretation, Friedman still does not support the rejection.

Among other differences between the Friedman circuit of Figure 5 and the invention is that in the invention the selector circuit provides a re-timed signal to a second exclusive OR circuit. The output of the unnumbered selector of Friedman, producing signal 533, is applied as a clock signal to the latches in the circuit 521 of Figure 5 of Friedman. See

paragraph [0077] of Friedman. That circuit is identified as a modified double-edge-triggered data flip-flop. See paragraph [0031] of Friedman. Further, as acknowledged in the Office Action, the inverted phase comparison polarity is missing in Friedman as are the one-pulse delay circuit and the latch delay circuit.

Ono fails to suggest any modification of Friedman that could produce the invention claimed. Ono does describe a clock signal correction circuit that employs circuits having names similar to the circuits of claim 1 that are missing from Friedman. However, that similarity is not sufficient to suggest the invention defined by claim 1. There is no description in Ono as to how the delay unit 22 could furnish both the latch delay circuit and the one-pulse delay circuit of the invention. Further, there is no description as to how those circuits would be interconnected with respect to the input signal and the second exclusive OR circuit, in combination with the unnumbered selector of Figure 5 of Friedman. The generalized assertion that it would have been obvious to one skilled in the art to borrow from Ono to modify Friedman to produce the claimed invention is not supported by the record.

Applicant acknowledges that, according to the description of Ono, the delay unit 22 provides a delay of one-half the cycle time of the input clock signal. Further, Ono describes the logical operator 23 as an exclusive OR operation. However, that logical operator does not receive the same signals received by the second exclusive OR circuit of claim 1 and, therefore, does not perform the same operation. Moreover, if it is asserted that the delay unit 22 of Ono corresponds to the one-pulse delay circuit of claim 1, then the latch delay circuit of the claimed circuit is still missing from the purported modification of Friedman with Ono. Finally, the purpose of Ono is not to correct clock phase as in the invention but to produce a duty ratio of 50%. See paragraph [0035] of Ono. That goal and its achievement in Ono are substantially different from the goal of the invention and the means by which that goal is achieved in the invention. These factors all show that Friedman cannot be modified by Ono to suggest the invention. In other words, *prima facie* obviousness has not been demonstrated because (i) all of the elements of claim 1 cannot be found in the asserted combination of Friedman and Ono, even as modified by Cai, and (ii) the interconnections, operations, and results of the invention and the purported combination of references are not the same.

Reconsideration and allowance of claim 1, along with its dependent claims 2-7, are earnestly solicited.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

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